ABSTRACT OF THE DISCLOSURE

A semiconductor memory testing implementation suitable for use in built-in self repair (BISR) memories provides advantages over conventional memory testing techniques. According to an embodiment, a memory testing circuit configuration includes an output register for receiving digital data. A plurality of shift registers serially output the digital data to be received by the output register. Each one of the plurality of shift registers includes a feedback path for enabling the digital data output by a corresponding one of the plurality of shift registers to be input back into the corresponding shift register in a same sequence as the digital data is output from the corresponding shift register.